WHAT IS CLAIMED IS:

1. A read circuit of a nonvolatile semiconductor memory comprising:

at least one sense amplifier; and

a read control signal generating circuit for supplying a first signal to said at least one sense amplifier,

wherein said at least one sense amplifier has a first current path comprised of a first P-channel MOS transistor having a source electrically connected to a first power supply node and a gate applied with said first signal, and a first N-channel MOS transistor connected between a drain of said first P-channel MOS transistor and a memory cell and having a gate applied with a second signal, and

said read control signal generating circuit has a second current path comprised of a second P-channel MOS transistor having a gate and a drain connected to the gate of said first P-channel MOS transistor and a source electrically connected to said first power supply node, and a second N-channel MOS transistor connected between the drain of said second P-channel MOS transistor and a reference cell and having a gate applied with said second signal.

2. The read circuit according to claim 1, wherein assuming that a write state is defined as a state in which a difference (Vcg-Vtcell) between a voltage Vcg at a control gate of said memory cell and a threshold voltage Vtcell is negative, and an erasure state is defined as a state in which said difference is positive, the sizes of said first and second P-channel MOS transistors and the value of a cell current of said reference cell are determined such that a drain current of said first P-channel MOS transistor is smaller than a cell current of said memory cell when said memory cell is in the erasure state.

3. The read circuit according to claim 2, wherein said first and second P-channel MOS transistors are sized in a ratio such that the value of the cell current of said reference cell is equal to the value of the cell current of said memory cell when said memory cell is in the

erasure state, and the value of the drain current of said first P-channel MOS transistor is one half of the value of the cell current of said reference cell.

4. The read circuit according to claim 1, wherein assuming that the number of said at least one sense amplifier is N, where N is a natural number, the number of said first P-channel MOS transistors is N, and said reference cell comprises M cells connected in parallel with each other, where M is a natural number and satisfies $M > N/4$.

5. The read circuit according to claim 1, wherein said reference cell has the same structure as a structure obtained by short-circuiting a control gate electrode to a floating gate electrode of said memory cell.

6. The read circuit according to claim 5, wherein a potential applied to a control gate electrode of said reference cell is set to a value such that a cell current of said reference cell is substantially equal to a cell current of said memory cell in an erasure state.

7. The read circuit according to claim 1, wherein for monitoring a threshold voltage of said memory cell having a negative threshold voltage in a test operation, a potential at a control gate electrode of said memory cell is fixed to a value for a normal read operation, and a potential at a control gate electrode of said reference cell is varied to detect the threshold voltage of said memory cell; and

for monitoring a threshold voltage of said memory cell having a positive threshold voltage, the potential at the control gate electrode of said reference cell is fixed to the value for the normal read operation, and a potential at the control gate electrode of said memory cell is varied to detect the threshold voltage of said memory cell.

8. The read circuit according to claim 1, wherein said at least one sense amplifier includes an inverter which functions as a sense circuit;

said inverter is comprised of a third P-channel MOS transistor having a gate applied with a fourth signal, a source connected to said first power supply node, and a drain

connected to an output node; and a third N-channel MOS transistor having a gate connected to a connection node between said first P-channel MOS transistor and said first N-channel MOS transistor, a source connected to a second power supply node, and a drain connected to said output node; and

said inverter discriminates data in said memory cell by detecting a change in a potential at said connection node.

9. The read circuit according to claim 8, wherein said connection node is precharged to a potential lower than a threshold voltage of said inverter before a sense operation.

10. The read circuit according to claim 1, wherein said read control signal generating circuit includes a precharge circuit, said precharge circuit precharging a first connection node between said second P-channel MOS transistor and said second N-channel MOS transistor, and a second connection node between said second N-channel MOS transistor and said reference cell, respectively, for a period other than a first period in which a cell current is flowing into said reference cell.

11. The read circuit according to claim 10, wherein a potential at said first connection node in a second period is set to a value identical to or lower than the potential at said first connection node in said first period, and a potential at said second connection node in said second period is set to a value identical to or lower than the potential at said second connection node in said first period.

12. The read circuit according to claim 1, wherein said at least one sense amplifier includes an N-channel MOS transistor which is connected in parallel with said first N-channel MOS transistor, and transitions to an ON state when a bit line is precharged.

13. The read circuit according to claim 1, wherein a potential on a bit line is reset before said bit line is precharged.

14. The read circuit according to claim 13, wherein a precharge period is provided for said bit line subsequent to a reset period for said bit line, said bit line being selected in the reset period of said bit line.

15. The read circuit according to claim 13, wherein the gate of said first N-channel MOS transistor is connected to said first power supply node when said bit line is precharged.